## REMARKS

Applicants respectfully request reconsideration of this application in view of the foregoing amendments and the following remarks.

**Claim Status**

Claims 1-12 are pending in this application and have been rejected. Claims 1-3 and 7-12 are herein amended. Claims 13 and 14 are herein added. No new matter has been added by these amendments.

**Rejections Under 35 U.S.C. § 103**

Claims 1-5 and 7-11 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,942,553 (Dalrymple) in view of U.S. Patent No. 6,748,497 (Kang).

Applicants respectfully submit that Dalrymple, when taken alone or in combination with Kang, does not disclose or suggest a computer system comprising a central processing unit (CPU) core; a digital signal processing (DSP) core; a data cache; a first buffer module for storing input data received by the DSP core; and a second buffer module for storing output data provided from the DSP core; wherein the input and output data are received by and provided from the DSP core in series through the first and second buffer modules without going through the data cache. See e.g., Fig. 2 and ¶0009 of Applicants' disclosure.

Claim 1 as amended recites, a computer system comprising:

> a central processing unit (CPU) core for executing instructions;
>
> a digital signal processing (DSP) core for processing data in accordance with the instructions;

a data cache for storing temporary data associated with the DSP core;

a first buffer module for storing input data received by the DSP core;

a second buffer module for storing output data provided from the DSP core; and

an external memory for storing the temporary data, the input data, and the output data,

wherein the input and output data are received by and provided from the DSP core in series through the first and second buffer modules without going through the data cache.

With regard to the rejection of claim 1, the Examiner indicated that Dalrymple discloses all the features recited therein, except the "data cache". To cure this deficiency in Dalrymple, the Examiner indicated that Kang "describes a system on a chip (Kang's Fig 2: #102 SOC) having microprocessor core (Kang's Fig 2: #128 corresponds to the claim's DSP core) and cache memory (Kang's Fig 2: #126, column 3 lines 53-65)."

Thus, according to the Examiner, it would have been obvious to one of ordinary skill in the art to "include the cache memory as suggested by Kang in Dalrymple's system thereby providing a fast access to data stored in the cache."

Although the Examiner is correct in indicating that Dalrymple does not disclose the claimed data cache, Applicants respectfully disagree with the Examiner's assertion that all of the other claim elements are disclosed therein. For example, in contrast to the Examiner's assertion that the microprocessor 102 is a DSP core, Applicants direct the Examiner to col. 4, lines 28-32 of Dalrymple which clearly indicate that the microprocessor 102 is a CPU. In other words, the microprocessor 102 is not a DSP core. Since the microprocessor 102 is not a DSP core, Dalrymple does not disclose the claimed buffer modules which serially store input and output data received by and provided from the DSP core. In addition, Applicants respectfully disagree with the Examiner's assertion

that the direct memory access (DMA) controller 104 (or coprocessor) is a CPU core. Instead, the DMA controller 104 (or coprocessor) is a device which allows access to a memory 106 independently of the CPU 102; the DMA controller 104 (or coprocessor) is not a CPU core. See e.g., Fig. 2 and col. 4, lines 28-43 of Dalrymple.

With regard to Kang, although Kang discloses a DSP engine 118 (e.g., a DSP core) in Fig. 1 thereof, Kang does not disclose the claimed first and second buffer modules that serially store input and output data received by and provided from the DSP core without going through the data cache. Instead, Kang discloses a buffer 136 for buffering memory transactions between the DSP engine 118 and a memory 126, which has been indicated by the Examiner as being the claimed data cache. See e.g., Fig. 1 and col. 4, lines 9-11 of Kang.

Accordingly, Applicants believe that the embodiment of the present invention as recited in amended claim 1 is patentable over the cited art of record because Dalrymple, either taken alone or in combination with Kang, does not disclose or suggest the embodiment of the invention as recited therein.

Claim 6 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Dalrymple in view of Kang and further in view of U.S. Patent No. 6,912,638 (Hellman). Claim 6 is believed to be allowable for at least the reasons discussed above for claim 1.

Claim 12 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Dalrymple in view of Kang and further in view of Hellman.

Similarly to claim 1, claim 12 has been amended to recite, *inter alia*, that "the input and output data are accessed in series without passing through the data cache". As

such, claim 12 is believed to be allowable for at least the reasons discussed above for claim 1.

**Amendments to Claims 2, 3 and 7-11**

Claim 2 has been amended to recite that the first and second buffer modules comprise an "address register". Claim 2 is believed to be allowable for at least the reasons discussed above for claim 1.

Claim 3 has been amended to recite that the address of the external memory is "set" by the CPU core. Claim 3 is believed to be allowable for at least the reasons discussed above for claim 1.

Claims 7 and 8 have been amended to bring them into conformity with the amendments to claim 1 from which they depend and are believed to be allowable for at least the same reasons.

Claims 9 and 10 have been amended to clarify that the auto-fill and auto-flush operations are carried out by the DSP core, respectively. Claims 9 and 10 are believed to be allowable for at least the reasons discussed above for claim 1.

Claim 11 has been amended to bring it into conformity with the amendments to claim 1 from which it depends and is believed to be allowable for at least the same reasons.

**New Claims 13 and 14**

Claim 13 has been added to further clarify that "the buffer of the first and second buffer modules is a sequential buffer". Claim 13 is believed to be allowable for at least the reasons discussed above for claim 1.

Claim 14 has been added to further clarify that "the auto-fill and the auto-flush operations are performed by the DSP core and the pre-fill and the post-flush operations are performed by the CPU core". Claim 14 is believed to be allowable for at least the reasons discussed above for claim 12.

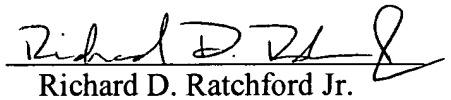
**Dependent Claims**

Applicants have not independently addressed the rejections of all the dependent claims because Applicants submit that, in view of the amendments to the claims presented herein and, for at least similar reasons as why the independent claims from which the dependent claims depend are believed allowable as discussed, supra, the dependent claims are also allowable. Applicants however, reserve the right to address any individual rejections of the dependent claims should such be necessary or appropriate.

## CONCLUSION

Accordingly, Applicants submit that the claims as herein presented are allowable over the prior art of record, taken alone or in combination, and that the respective rejections be withdrawn. Applicants further submit that the application is hereby placed in condition for allowance which action is earnestly solicited.

Respectfully submitted,

By: 

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